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REMARKS / DISCUSSION OF ISSUES

Claims 1-20 are pending in the application.

The applicant thanks the Examiner for acknowledging the claim for priority and receipt of certified copies of all the priority documents, and for determining that the drawings are acceptable.

The applicant thanks the Examiner for providing information about recommended section headings. However, the applicant respectfully declines to add the headings. Section headings are not statutorily required for filing a non-provisional patent application under 35 USC 111(a), but are only guidelines that are suggested for applicant's use. (See Miscellaneous Changes in Patent Practice, Response to comments 17 and 18 (Official Gazette, August 13, 1996) [Docket No: 950620162-6014-02] RIN 0651-AA75 ("Section 1.77 is permissive rather than mandatory. ... [T]he Office will not require any application to comply with the format set forth in 1.77").

The Office action rejects claims 1-2, 4-5, and 19 under 35 U.S.C. 102(b) over Kasperkovitz (WO 01/58029). The applicant respectfully traverses this rejection.

The Examiner's attention is requested to MPEP 2131, wherein it is stated:

"A claim is anticipated only if *each and every element* as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). "The *identical invention* must be shown in as *complete detail* as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Claim 1, upon which claims 2-6 and 15-20 depend, claims a mirror suppression circuit that includes a quadrature output of an error correction circuit that is coupled through a first filter circuit for a selection of the quadrature signal to a first quadrature input of an error detection circuit, and coupled prior to the first filter circuit through a second quadrature signal path to a second quadrature input of the error detection circuit, wherein the error detection circuit provides amplitude and phase

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control signals that vary with I_w*I_{ref} and Q_w*Q_{ref}, and I_w*Q_{ref} and Q_w*I_{ref}, respectively, and:

I_w and Q_w representing the signals at the first quadrature input of the error detection circuit, and

I_{ref} and Q_{ref} representing the signals at the second quadrature input of the error detection circuit.

Claim 7, upon which claims 9-14 depend, includes similar limitations.

Kasperkovitz fails to teach a quadrature output of an error correction circuit that is coupled through a first filter circuit to a first quadrature input of an error detection circuit and coupled prior to the first filter circuit to a second quadrature input of the error detection circuit.

Kasperkovitz teaches that the quadrature output of the error correction circuit 10 is provided to a demodulator 4, and to an error detection circuit 11. The applicant respectfully maintains that a demodulator is not a filter, per se. Kasperkovitz's demodulator 4 includes a filter 9, but this filter 9 does not receive a quadrature input, nor does it provide a quadrature output that is provided to the error detection circuit 11.

Assuming in argument that a demodulator can be considered equivalent to a filter, the applicant further notes that Kasperkovitz's error detection circuit 11 does not correspond to the applicant's claimed error detection circuit.

Kasperkovitz's error detection circuit 11 detects an error amount based on the quadrature output of VCO 7 in demodulator 4 and the quadrature output of the VCO 20 in demodulator 12. The applicant's error detection circuit EDC, on the other hand, detects an error amount based on a filtered version Idi1, Idq1 of the quadrature output Oci, Ocq of the error correcting circuit ECC, and an inverted unfiltered version Idi2, Idq2 of the same quadrature output Oci, Ocq.

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Comparing Kasperkovitz's circuit to the claimed circuit elements of claims 1 and 7 in specific detail, the two quadrature inputs to Kasperkovitz's error detection circuit 11 are the quadrature outputs from the error control circuit 10 that enter on the left side of circuit 11 in Kasperkovitz's FIG. 1, and the quadrature outputs from the demodulator 4 that enter the top of circuit 11, labelled Iw and Qw. Kasperkovitz teaches that the error detection circuit provides outputs based on $I_w{}^*I_U$ and $Q_w{}^*Q_U$, and $I_w{}^*Q_U$ and $Q_w{}^*I_U$.

The applicant specifically claims that the error detection circuit provides outputs based on $I_w{}^*I_{ref}$ and $Q_w{}^*Q_{ref}$, and $I_w{}^*Q_{ref}$ and $Q_w{}^*I_{ref}$; wherein I_w and Q_w representing the signals at the first quadrature input of the error detection circuit, and I_{ref} and Q_{ref} representing the second quadrature input of the error detection circuit. Thus, for the applicant's claimed invention to be equivalent to Kasperkovitz, Kasperkovitz's signals Iu and Qu must correspond to the applicant's claimed signals Iref and Qref.

The applicant specifically claims that the signals Iref and Qref are the signals applied to the second quadrature input of the error detection circuit. Thus, to establish equivalence, Kasperkovitz's signals Iu and Qu must correspond to the second quadrature input of the error detection circuit 11. As noted above, in establishing a correspondence of structure to the applicant's claimed structure, the output of Kasperkovitz's error correction circuit 10 corresponds to the second quadrature input of the error detection circuit 11. As is clear in Kasperkovitz's FIG. 1, the outputs of Kasperkovitz's error correction circuit 10 are not the signals Iu and Qu; as noted above, Kasperkovitz's signals Iu and Qu are the outputs of the VCO 20, and not inputs to the error detection circuit 11. Thus, Kasperkovitz's signals Iu and Qu cannot be said to correspond to the applicant's claimed signals Iref and Qref.

Because Kasperkovitz fails to teach each of the elements of the applicant's claimed invention, the applicant respectfully maintains that the rejection of claims 1-2, 4-5, and 19 under 35 U.S.C. 102(b) over Kasperkovitz is unfounded, per MPEP 2131.

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The Office action rejects:

claims 3, 6, 15-18, and 20 under 35 U.S.C. 103(a) over Kasperkovitz and Komarek (USP 6,408,008); and

claim 4 under 35 U.S.C. 103(a) over Kasperkovitz and Leyonhjelm (WO 99/23756).

MPEP 2142 states:

"To establish a *prima facie* case of obviousness … the prior art reference (or references when combined) ***must teach or suggest all the claim limitations***… If the examiner does not produce a *prima facie* case, the applicant is under no obligation to submit evidence of nonobviousness."

Each of the rejected claims 3-4, 6, 15-18, and 20 are dependent upon claim 1. In these rejections, the Office action relies upon Kasperkovitz for teaching the elements of claim 1.

As noted above, Kasperkovitz fails to teach each of the elements of claim 1, and thus the applicant respectfully maintains that the rejections of claims 3-4, 6, 15-18, and 20 under 35 U.S.C. 103(a) that rely upon Kasperkovitz for this teaching is unfounded, per MPEP 2142.

The Office action rejects claim 7 under 35 U.S.C. 103(a) over Kasperkovitz, Walton et al. (USP 7,054,378), and Leyonhjelm. The applicant respectfully traverses this rejection.

As noted above, claim 7 includes the limitations of claim 1, and Kasperkovitz fails to teach the elements of claim 1.

Because Kasperkovitz fails to teach each of the elements of claim 7, the applicant respectfully maintains that the rejections of claim 7 under 35 U.S.C. 103(a) is unfounded, per MPEP 2142.

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In view of the foregoing, the applicant respectfully requests that the Examiner withdraw the rejections of record, allow all the pending claims, and find the application to be in condition for allowance. If any points remain in issue that may best be resolved through a personal or telephonic interview, the Examiner is respectfully requested to contact the undersigned at the telephone number listed below.

Respectfully submitted,

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